Remarks

Claims 1-7 and 12-21 are pending in the application and are presented for reconsideration. Claims 1-7 have been amended; claims 12-21 have been added. No new matter has been added.

Support for the amendments to the claims 1-7 may be found in the specification at page 8, lines 2-3 and 16-19.

Claim Rejections

Claims 1, 3-4, and 7 are rejected under 35 U.S.C. § 102(b) as being anticipated by US Patent No. 5,036,222 to Davis.

Claims 2 and 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,036,222 to Davis in view of US Patent No. 5,877,647 to Vajapey et al.

In view of the amendments made herein, the Examiner's rejections of the claims are respectfully traversed.

I. Rejections of Claims Under 35 U.S.C. § 102

1. Legal standard for Rejecting Claims Under 35 U.S.C. §102

Under 35 U.S.C. § 102, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros., Inc. v. Union Oil Co.*, 814 F.2d 628 (Fed. Cir.), *cert. denied*, 484 U.S. 827 (1987).

2. Response to 35 U.S.C. § 102 Rejections

a. Claims 1, 3-4, and 7

Claim 3 now recites:

> An apparatus for reducing the slew rate of transition edges of a digital signal on a node of an integrated circuit, comprising:
> a first switchably conductive device characterized by a first threshold voltage, said first switchably conductive device connected

between said node and a voltage source and having a control input connected to a driving signal to allow current conduction from said voltage source to said node when a voltage level of said driving signal is equal to and greater than said first threshold voltage and to disallow said current conduction when said voltage level of said driving signal is less than said first threshold voltage; and

a second switchably conductive device characterized by a second threshold voltage greater than said first threshold voltage, said second switchably conductive device connected between said node and said voltage source and having a control input connected to said driving signal to allow current conduction from said voltage source to said node when a voltage level of said driving signal is equal to and greater than said second threshold voltage and to disallow said current conduction when said voltage level of said driving signal is less than said second threshold voltage.

The Examiner seeks to make the following equivalences: a first switchably conductive device N1 characterized by a first threshold voltage (the voltage which starts to turn ON transistor N1), said first switchably conductive device connected between said node VOUT and a voltage source GROUND and responsive to a driving signal (VIN, or also signal at gate of N1) to allow current conduction from said voltage source to said node when said driving signal is offset from said voltage source by a voltage equal to and greater than said first threshold voltage and to disallow said current conduction when said driving signal is offset from said voltage source by a voltage less than said first threshold voltage (when VIN changes, VOUT changes, and when VIN changes to a first certain voltage, transistor N1 is ON first, the first threshold voltage is the VIN voltage at this first moment, and when the voltage of VIN is less than this first threshold voltage the current conduction is disallowed through N1, col. 10, lines 16-36); and

a second switchably conductive device (transistors N3 and P4) characterized by a second threshold voltage (the VIN voltage which starts to turn ON transistor N3) greater than said first threshold voltage (col. 10, line 35, i.e., two steps or "bifurcated turn on"), said second switchably conductive device connected between said node and said voltage source and responsive to said

driving signal to allow current conduction from said voltage source to said node when said driving signal is offset from said voltage source by a voltage substantially equal to and greater than said second threshold voltage and to disallow said current conduction when said driving signal is offset from said voltage source by a voltage less than said second threshold voltage (VIN keeps changing, VOUT also keeps changing accordingly, and when VIN changes to a second certain voltage, transistor N3 is ON, the second threshold voltage is the VIN voltage at this second moment, and when the voltage of VIN is less than this second threshold voltage, the current conduction is disallowed through N3).

Claim 3 has been amended to recite that each of the first and second switchably conductive devices includes a control input, both of which are commonly driven by a single driving signal. In view of this amendment, the Applicant respectfully traverses the rejection of claim 3 under 35 U.S.C. § 102(b).

Davis does not meet the limitations of amended claim 3. In formulating the rejection of claim 3, the Examiner seeks to equate Davis's transistor combination P4 and N3 with Applicant's "second switchably conductive device characterized by a second threshold voltage greater than said first threshold voltage", and Davis' VIN to Applicant's "driving voltage". Under this equivalence, the control input of Davis' first switchably conductive device is the gate of N1. Further the control input of Davis' second switchably conductive device is the gate of P4 (since N3 cannot turn on until P4 is first turned on via presenting a low signal at the gate of P4). However, as clearly shown in Davis, FIG. 2, VIN is not connected to either the gate of N1 or the gate of P4. Accordingly, VIN cannot be equated to the "driving signal" since such equivalence does not meet the limitation "a first switchably conductive device ... having a control input connected to a driving signal" and "a second switchably conductive device ... having a control input connected to said driving signal".

In addition, the signal present on the gate of N1 also cannot be equated with the "driving signal" recited in Applicant's claim 3 for the reason that the signal present on the gate of N1 is not also connected to the gate of P4. Thus,

this equivalence also does not meet the limitation "a second switchably conductive device ... having a control input connected to said driving signal".

Furthermore, there is no other signal in Davis that can be equated with Applicant's "driving signal" that meets the limitations of Claim 3.

In summary, Davis does not meet the limitations of Applicant's claim 3, including "a second switchably conductive device characterized by a second threshold voltage greater than said first threshold voltage, said second switchably conductive device connected between said node and said voltage source and having a control input connected to said driving signal to allow current conduction from said voltage source to said node when a voltage level of said driving signal is equal to and greater than said second threshold voltage and to disallow said current conduction when said voltage level of said driving signal is less than said second threshold voltage". Per *Verdegaal Bros., Inc. v. Union Oil Co., supra*, since Davis does not teach each and every element as set forth in claim 3, Davis cannot be used in formulating a rejection under 35 U.S.C. § 102(b). Accordingly, the Applicant respectfully requests the Examiner to withdraw the rejection.

As per claim 4, claim 4 recites the same limitations as claim 3 and adds additional limitations. For the same reasons that Davis does not meet the limitations of claim 3, Davis also does not therefore meet the limitations of claim 4. Accordingly, the Applicant respectfully submits that the rejection of claim 4 under 35 U.S.C. § 102(b) should be withdrawn.

Claim 4 is believed allowable on independent grounds in that none of the references teach or suggest the limitation "wherein said first switchably conductive device comprises a single field effect transistor (FET) and said second switchably conductive device comprises a single field effect transistor (FET)". In other words, none of the references teach two single FET devices, each characterized by different threshold voltages, each having a source connected to a common source and a drain connected to a common node, and each commonly driven by a single driving signal at their gates.

As per claim 1, claim 1 recites similar limitations as claim 3, in method form. For the same reasons that Davis does not meet the limitations of claim 3, Davis also does not therefore meet the limitations of claim 1. Accordingly, the Applicant respectfully requests that the Examiner withdraw the rejection of Claim 1.

As per claim 2, claim 2 recites the same limitations as claim 1 and adds additional limitations. For the same reasons that Davis does not meet the limitations of claim 1, Davis also does not therefore meet the limitations of claim 2. Accordingly, the Applicant respectfully requests that the Examiner withdraw the rejection of Claim 2.

As per claim 7, claim 7 recites similar limitations as claim 3. For the same reasons that Davis does not meet the limitations of claim 3, Davis also does not therefore meet the limitations of claim 7. Accordingly, the Applicant respectfully requests that the Examiner withdraw the rejection of Claim 7.

II. Rejections of Claims Under 35 U.S.C. § 103

1. Response to Rejections of Claims Under 35 U.S.C. § 103

The Applicant repeats all of the arguments presented with respect to Davis, Vajapey, and Kaplinsky in the prosecution history to date. As presented in those arguments, neither Vajapey, Kaplinsky, nor any of the other prior art of record makes up for the deficiencies of Davis with respect to Claim 3. Accordingly, Claim 3 could not be construed as being obvious over the prior art of record.

As per claim 5, claim 5 recites the same limitations as claim 3 and adds additional limitations. The limitations of claim 5 are not met for the same reasons that the limitations of claim 3 are not met by Davis, nor any of the other prior art of record taken in any combination. Accordingly, the Applicant respectfully requests the Examiner to withdraw the rejection of Claim 5.

As per claim 6, claim 6 recites the same limitations as claim 3 and adds additional limitations. The limitations of claim 6 are not met for the same reasons

that the limitations of claim 3 are not met by Davis, nor any of the other prior art of record taken in any combination. Accordingly, the Applicant respectfully requests the Examiner to withdraw the rejection of Claim 6.

As presented in the arguments presented with respect to Davis, Vajapey, and Kaplinsky in the prosecution history to date, neither Davis, Vajapey, Kaplinsky, nor any of the other prior art of record, taken in any combination, makes up for the deficiencies of Davis with respect to claim 1. Accordingly, Claim 1 could not be construed as being obvious over the prior art of record, and therefore the Applicant respectfully requests the Examiner to withdraw the rejection of Claim 1.

As per claim 2, claim 2 recites the same limitations as claim 1 and adds additional limitations. The limitations of claim 2 are not met for the same reasons that the limitations of claim 1 are not met by Davis, nor any of the other prior art of record taken in any combination. Accordingly, the Applicant respectfully requests the Examiner to withdraw the rejection of Claim 2.

II. Addition of Claims 12-21

Claims 1-7 were amended to more specifically set forth the condition of switchably conductive devices that turn on when a driving signal presented at their control input turn on only when the driving signal reaches or exceeds the characteristic threshold voltage of the given device (e.g., NFET transistors). Support for these amendments may be found in the Application at least at FIG. 2 (N_{LV} and N_{HV}) and in the Specification at least at page 6, lines 7-12 and page 7, line 25-32.

Claims 12-18 were added to cover the condition of switchably conductive devices that turn on when a driving signal presented at their control input turn on only when the driving signal is less than or equal to the characteristic threshold voltage of the given device (e.g., PFET transistors).

Support for these claims may be found in the Application at least at FIG. 2 (P_{LV} and P_{HV}) and in the Specification at least at page 6, lines 3-6 and 26-28.

Claims 19-21 were added to more specifically cover the circuit structure of the embodiment shown in FIG. 2 of the application.

Support for these claims may be found in the Application at least at FIG. 2 (P_{LV}, P_{HV} and N_{LV}, N_{HV}) and in the Specification at least at page 6, lines 3-12 and 26-28, and page 7, line 25-32.

None of the references cited teach or suggest the essential limitations of Applicant's claims 12-18.

The application is now believed to be in condition for allowance.

Conclusion

In view of the foregoing remarks, it is respectfully submitted that none of the references cited by the Examiner taken alone or in any combination shows, teaches, or discloses the claimed invention, and that Claims 1-7 and 12-21 are in condition for allowance. Reexamination and reconsideration are respectfully requested.

Should the Examiner have any questions regarding this amendment, or should the Examiner believe that it would further prosecution of this application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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Jessica J. Costa, Reg. No. 41,065

The Law Offices of Jessica Costa, PC
501 Collings Avenue
Collingswood, New Jersey 08107
Tel.: (856) 854-3999
Fax: (856) 858-2167